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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,556	02/19/2004	Yoshihiko Takagi	NGB-36462	5147
116	7590	10/10/2008	EXAMINER	
PEARNE & GORDON LLP 1801 EAST 9TH STREET SUITE 1200 CLEVELAND, OH 44114-3108			BAYOU, YONAS A	
			ART UNIT	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

<b>Application No.</b> 10/782,556	<b>Applicant(s)</b> TAKAGI ET AL.	
<b>Examiner</b> YONAS BAYOU	<b>Art Unit</b> 2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1)  Responsive to communication(s) filed on 19 February 2004.
- 2a)  This action is **FINAL**.                      2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4)  Claim(s) 1-15 and 17 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) \_\_\_\_\_ is/are allowed.
- 6)  Claim(s) 1-15 and 17 is/are rejected.
- 7)  Claim(s) \_\_\_\_\_ is/are objected to.
- 8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on 17 May 2004 is/are: a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \*    c)  None of:
1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5)  Notice of Informal Patent Application
- 6)  Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This office action is in response to applicant's response filed on 06/02/2008.
2. Claims 1-15 and 17 are pending.
3. Claims 1 and 13 are amended.
4. Claim 16 is cancelled.
5. Applicant's arguments have been fully considered but they are not persuasive.

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/02/2008 has been entered.

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-15 and 17 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iguchi et al., Pub. No.: US 2002/0169960 A1 in view of Shiraki et al., Patent No.: 5,892,979.

Referring to claims 1 and 13, Iguchi teaches a memory device comprising:  
a first tamper resistant memory which cannot be accessed directly by external electronic device [**abstract, para. 4 and figs. 1 and 5**; the high-security data into the tamper-resistant module is encrypted]; and

a second non-tamper resistant memory which cannot be directly accessed by external electronic device [**abstract, para. 50 and figs. 1 and 5**; flash memory 140 is corresponding to a second non-tamper resistant memory], Iguchi further teaches: wherein data stored in the first memory is saved to the second memory [**paras. 13-15 and 48**]. Iguchi does not appear to teach explicitly, wherein if there is no space area for downloading or installing data in the first memory, arbitrary data which is accumulated in the first memory and possible to

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be saved is saved to the second memory, and wherein the saved data is restored in the first memory when there is space area available in the first memory.

However, Shiraki teaches in fig. 15, overflow control unit 2030 has its sequencer 2032 perform the following determinations (A) through (E). (A) When processor 100 issues a write-in request for writing packet data into a queue, i.e. FIFO buffer unit 1010, overflow control unit 2030 has its sequencer 2032 determine whether or not saving buffer 1020 has an available space, according to whether or not Full 3 signal inputted from pointer comparator 2031 is active. (B) By referring to flag data set in flag 1032, and by determining whether or not flag 1032 is set, overflow control unit 2030 has its sequencer 2032 determine whether or not saving buffer 1020 currently saves overflowed data. A positive determination causes overflow control unit 2030 to have its sequencer 2032 determine next the status of Full 2 signal from FIFO buffer unit 1010, thereby determining whether or not FIFO buffer unit 1010 currently has an available space. (C) If determination (A) ascertains that saving buffer 1020 currently has an available space, overflow control unit 2030 has its sequencer 2032 determine whether or not overflow flag 1032 is set, i.e. whether or not FIFO buffer unit 1010 has available space. As described above, flag 1032 being set means that saving buffer 1020 currently saves data. (D) If determination (A) ascertains that saving buffer 1020 currently has an available space, overflow control unit 2030 has its sequencer 2032 determine whether or not flag 1032 is reset and FIFO buffer unit 1010 has an available space. (E) Upon determining that neither a condition for performing determination (A) nor a condition for performing determination (B) exist at a

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START, overflow control unit 2030 has its sequencer 2032 repeat processes from START to START in a loop. Alternatively, when saving buffer 1020 has no available space, overflow control unit 2030 has its sequencer 2032 secure a new saving area for saving data therein **[17:30-67 and fig. 15]**; overflow control unit 2030 secure a new saving area for saving data when there is no space]. Iguchi and Shiraki are analogous art because both teach secured memory device.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Iguchi to include when saving buffer 1020 has no available space, overflow control unit 2030 has its sequencer 2032 secure a new saving area for saving data therein of Shiraki because overflow control unit 2030 has its sequencer 2032 write, into either one of FIFO buffer unit 1010 and saving buffer 1020, packet data about which processor 100 issues a write-in request to a queue, according to the determination results [18:1-6], please see *KSR International Co. v. Teleflex Inc.*, 550 U.S., 82 USPQ2d 1385 (2007) for further interpretation.

Referring to claims 2 and 5, Iguchi teaches a memory device comprising: wherein the saved data is data prepared when installing an application program or executing the application program **[abstract and para. 3]**.

Referring to claim 3, Iguchi teaches a memory device comprising: wherein when the data is saved to the second memory, the program code of the application program is rejected from the first memory **[para. 50]**.

Referring to claim 4, Iguchi teaches a memory device comprising: wherein when the data is saved to the second memory, the program code of the application program is left in the first memory **[para. 50]**.

Referring to claim 6, Iguchi teaches a memory device comprising: a managing table in which the managing information for the data stored in the first memory is described, wherein the managing information includes information indicating whether or not the data can be saved **[paras. 65, 76, 117 and figs. 17, 19C and 22]**.

Referring to claim 7, Iguchi teaches a memory device comprising: wherein the application program is downloaded in the first memory and installed in the first memory **[abstract, paras. 88, 106, 139 and figs. 13-14]**.

Referring to claim 8, Iguchi teaches a memory device comprising: wherein the application program is downloaded in the second memory and installed in the first memory **[abstract, paras. 106, 139 and figs. 13-14]**.

Referring to claim 9, Iguchi teaches a memory device comprising: wherein the application program is downloaded in the second memory and installed in the second memory **[abstract, paras. 88, 106, 139 and figs. 13-14]**.

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Referring to claim 10, Iguchi teaches a memory device comprising:  
wherein the saved data and the signature information for the data are encoded  
and saved to the second memory **[abstract, paras. 11, 41 and 50]**.

Referring to claim 11, Iguchi teaches a memory device comprising:  
wherein the first memory includes a saved information managing unit for  
managing saved information, data to be saved is encoded and saved, and the  
signature information of the encoded data is stored in the saved information  
managing unit **[abstract, paras. 50-51]**.

Referring to claim 12, Iguchi teaches a memory device comprising:  
wherein data to be saved is determined on the basis of an instruction from an  
electronic device **[abstract]**.

Referring to claim 14, Iguchi teaches a memory device comprising:  
wherein specific saved data is restored in accordance with a restoration  
instruction from the electronic device **[abstract, paras. 5 and 41]**.

Referring to claim 15, Iguchi teaches a memory device comprising:  
wherein the saved data related to the application program is restored in  
accordance with a start instruction of the application program from the electronic  
device **[abstract, paras. 116]**.



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Claim 16: Cancelled

Referring to claim 17, Iguchi teaches the memory device further comprising an inner CPU which can directly access to both the first memory and the second memory [**abstract, paras. 41 and 46**].

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YONAS BAYOU whose telephone number is (571)272-7610. The examiner can normally be reached on m-f,7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kambiz Zand can be reached on 571-272-3811. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yonas Bayou/

Examiner, Art Unit 2134

10/01/2008

/Kambiz Zand/

Supervisory Patent Examiner, Art Unit 2434